HDL DESIGN FOR BIST BASED IEEE BOUNDARY SCAN SOC ARRAY SCANNER ARCHTECTURE USING FPGA

PROF P.N.V.M SASTRY
J.B.R.E.C., Dean- R&D-CELL & ECE, Hyderabad, India
shastrypnvm@gmail.com

PROF G.KRISHNAIAH
J.B.R.E.C., Professor – ECE, Hyderabad ,India
krishh786@gmail.com

PROF.DR.D.N.RAO
J.B.R.E.C., Principal , Hyderabad, India
principal_jbr@yahoo.com

DR S.VATHSAL
J.B.I.E.T., Dean- R&D&EEE, Hyderabad, India
svathsal@gmail.com

ABSTRACT: The Aim is for Design Implementation Of IEEE 1149.1 Standard Based Boundary Scan B.I.S.TArray SOC Architecture for Testing of Multiple SOC's at a time for flexibility and compatibility. This DesignConsists Of Array Of BIST Modules Parallel. Testing Done Parallel by using these BIST Modules. "This isSimply a Parallel Test Computing Technique – Universal SOC Tester". The Process Of Design Implementedthrough VHDL & / Verilog HDL. Simulation & Synthesis Done By Xilinx ISE 9.2 i EDA Software DesignTool. Programming & Debugging Done By FPGA SPARTAN-III.

KEYWORDS: IEEE- International Institute of Electrical & Electronics Engineering, B.I.S.T - Built InSelf Test, SOC – System On Chip, JTAG- Joint Test Action Group, VHDL – Very High Speed IntegratedCircuit Hardware Description Languages, ISE – Integrated Software Environment, EDA – ElectronicDesign Automation.

INTRODUCTION

B.I.S.T is Defined as the "**Built In Self Test**" Industry Standard Test Automation Technique, Automatically Test / Configure the Design Data Of Multiple **SOC's / Cards**. Simply It is Called **SOC Programmer.** This **B.I.S.T** Array **SOC Architecture** Implemented By Soft Process Technique Using CPLD / FPGA **Configuration.** The purpose is to test multiple SOC's & Multi Channel Design Based High Speed Communication Protocols in terms of **Mbps/ Gbps** Data Rate Speed**. B.I.S.T** normally Consists of Three Modes Of Operation – Normal Mode, Scanning Mode, Test Mode (LFSR Mode). Normal Mode Simply General Register Operations. In Scanning Mode Scanning the Data Serially for **Parallel B.I.S.T Array SOC** Architecture. In the Test Mode, This BIST Array SOC Acts as Simply LFSR Operation. The Flexibility Of this LFSR BIST Array SOC is to test the Array Processor SOC's / Programmable SOC Cores by implementation of Parallel Distributed IEEE Boundary Scanning SOC Test Computing Technique of Different Pattern

Sequences. Simply This Architecture is almost similar to **MEMORY ARRAY COMPATIBLE BIST SOC** Architecture. Implementation of Testing Design on FPGA using IEEE JTAG Cable. JTAG Abbreviated as Joint Test Action Group Cable. Basically **B.I.S.T** Architecture Consists of **TAP Controller (Test Access Port** , Design Under Test, Test Response Analyzer, and Signature Register , TAP Controller Contains the Signals following – **TCLK, TMS , TDI, TDO, TRST. TCLK. TMS** Test Mode Selection selects the multiple test modes either serial / parallel**. TDI & TDO –** Test the Data Input & Output.

Boundary-scan design principles

The LSSD boundary-scan design method used for IBM CMOS ASICs is somewhat different from the proposed IEEE 1 149.1 boundary-scan architecture [4]. It is instructive, therefore, not only to explain the LSSD boundary-scan approach, but also to compare it with the IEEE 1 149. I approach. This can best be accomplished by first reviewing the essential elements of the 1 149. I architecture. The LSSD boundary-scan method is then introduced and contrasted with the proposed IEEE standard. IEEE 1149.1 boundary-scan The IEEE I 149.1 boundary-scan architecture requires that a standard test access port (TAP) be designed into each conforming component. The TAP is operated by means of a four-pin test-signal interface. The signal pins comprise a test clock (TCK), a test mode select (TMS), a serial test data input (TDI), and a serial test data output (TDO). illustrated in Figure 1. The test access port is controlled by an internal, synchronous finite-state machine consisting of sixteen states. Its prescribed behavior is governed by the values placed on the TMS input at the time of a rising edge transition on the TCK signal. The state machine is defined so that it can be initialized to a known reset state within six test clock cycles. (Note: IEEE 1 149.1 also defines an optional test reset signal that permits immediate, asynchronous initialization at the expense of an extra test pin.) The TAP is required to contain a serially loadable instruction register and a one bit scan bypass register. The 1149.1 method specifies that all component signal 1/0 pins (other than the test signal interface pins) must be directly connected to logically adjacent boundary-scan cells. Those cells must also be interconnected to form a single boundary-scan register operated under TAP control. The proposed standard defines three mandatory instructions: 1) BYPASS-to permit board-level shift register reconfiguration for more efficient scanning (using the bypass register); 2) EXTEST-to permit testing of board interconnect wiring (using the boundary-scan register); and 3) SAMPLE-to permit monitoring of signals entering and leaving a component during normal system operation (using the boundary-scan register). The basic 1 149.1 boundary-scan cell design is depicted in Figure 2. Some variations on this theme are permitted, but all 1 149.1-compatible cell designs must contain a multiplexor and latch combination in order to concurrently support both EXTEST and SAMPLE operation requirements. In EXTEST mode, the boundary-scan latches must be able to control all component output signals and monitor all component input signals. In SAMPLE mode, the boundary-scan latches must be able to simultaneously monitor all component functional input and output signals without impeding system functional signal flow. indicate that it is primarily intended to facilitate board assembly verification. The EXTEST operation permits simple scan testing of the interconnect wiring between boundary-scan components. This can be done without requiring either in-circuit tester access to all pins on all components (which SMT has made difficult) or a detailed description of each component's internal functional logic (which is generally unavailable for vendor VLSI catalog components). By contrast, the proposed standard does not require any internal system logic testing operation at all. It does recommend that one be provided, however, and defines the rules for optional instructions (RUNBIST and INTEST) to permit internal logic testing either by invoking built-in self-test facilities or by using the boundary-scan register to apply a vendor-supplied scan test.

LSSD boundary-scan

When a board is designed entirely with IBM LSSD components, a gate-level logic model of each component is available to the board designer. Thus, it is technically possible to automatically generate a test for the entire board, including its component interconnect wiring [1 11. However, if the component quality levels are uniformly high, the dominant failures encountered during board testing are due to faulty component mounting or interconnection, and not to internal component faults. In such cases, the effort required to generate and apply tests for those internal faults is not justified. Board testing efficiency can be substantially improved, though, by generating tests only for faults associated with the component pins and the board wiring. The test generation process can be simplified even further by minimizing the amount of board logic that must be analyzed in developing such tests. One way to do this would be to implement LSSD-compatible IEEE 1149.1 boundary-scan structures on each ASIC component (see Appendix A of [4]). Tests for the board interconnections could then be automatically generated and applied using the 1 149.1 EXTEST protocol, which permits all internal-component functional logic to be ignored. The ASKS could continue to be treated as ordinary LSSD designs during component testing, however, since the logic added for 1 149.1 compliance is indistinguishable from other functional logic for purposes of LSSD test generation.

LSSD boundary-scan design rules apply:

Rule 1 There must be a TFPI sensitizing condition, consistent with the LSSD scan state and scan sequence, that makes all internal logic signals, and all embedded random-access memory (RAM) or read-only memory (ROM) arrays, IBM J. RES. DEVELOP, VOL. 34 NO 213 MARCHIMAY 1990 Output mode control System data , I TO system P'n -Scan out Update DR controllable and observable using only the TFPIs, TFPOs, and SRLs.

Rule 2 There must be a TFPI sensitizing condition, consistent with the LSSD scan state and scan sequence, that makes all external logic signals, including all 1/0 pins (TFPIs, data PIS, TFPOs, and data POs), controllable and observable using only the BSRLs and the 1/0 pins themselves.

Rule 3 All logic signals must be included in either the internal region, the external region, or both and each possible value of a signal must be testable (Le., simultaneously controllable and observable) under at least one of the two sensitizing conditions.

SOFTWARE – VLSI IC DESIGN FLOW

Description: The Universal Boundary Scan SOC BIST Array Tester Testing the Functional ASIC Modules SOC,ASIC,MCM at time, for reduction of time consumption. Simply It is called IEEE 1149.1 Universal Boundary Scan SOC Array Tester based on the BIST Array ASIC IP Cores. Implementation Done through FPGA. This is very Hi-Fi SOC BIST ARRAY Scanner Tester for testing /Scanning of Large Complex SOC's Data and Large Computing Data Center Stations / Cloud/Cluster/Grid/Internet Data Computing Servers. These SOC's are Integrated on Single System On Chip and Testing Done through TAP Controller Test Access Port ,this Contains Test Clock, Test Data In, Test Data Out, Test Mode Selection, Test Reset for the SOC Array Reconfiguration. The IEEE Boundary Scan SOC Architecture Contains Boundary Scan SOC Cell Arrays , Boundary Scan Registers Instruction and Data. Parallel BIST Registers are used for Testing these SOC Arrays . This BIST Contains LFSR Data Register used to test the SOC Data. SOC's are tested through SCAN IN and SCAN out Shift Register. The SOC's Are act as a MACROCELLs for this case.

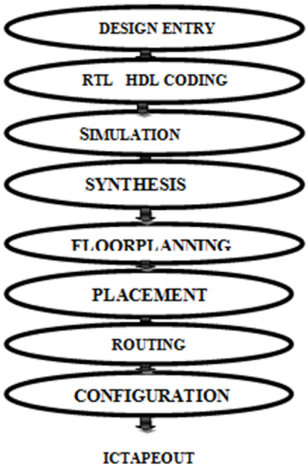

Figure 1. VLSI-EDA Software Design Flow Chart

B.I.S.T ARRAY SOC ARCHITECTURE

Unversal bist array soc tester architecture implementation

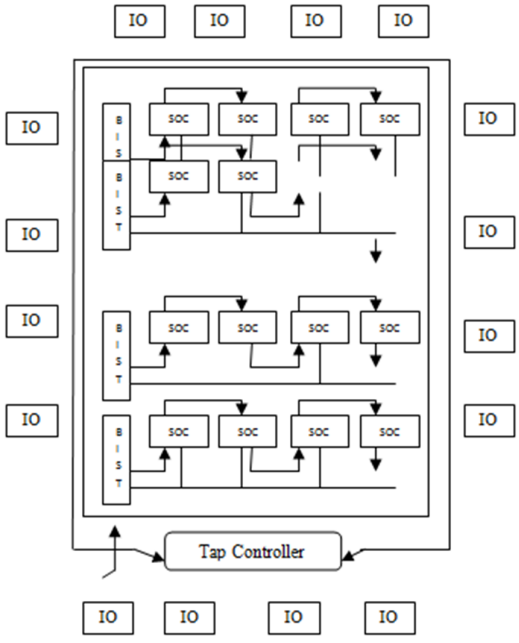

Figure 2. Universal Boundary Scan SOC BIST Array Tester

SIMULATION RESULTS –Universal BIST

SimulationResults- Universal BIST Array SOC Test

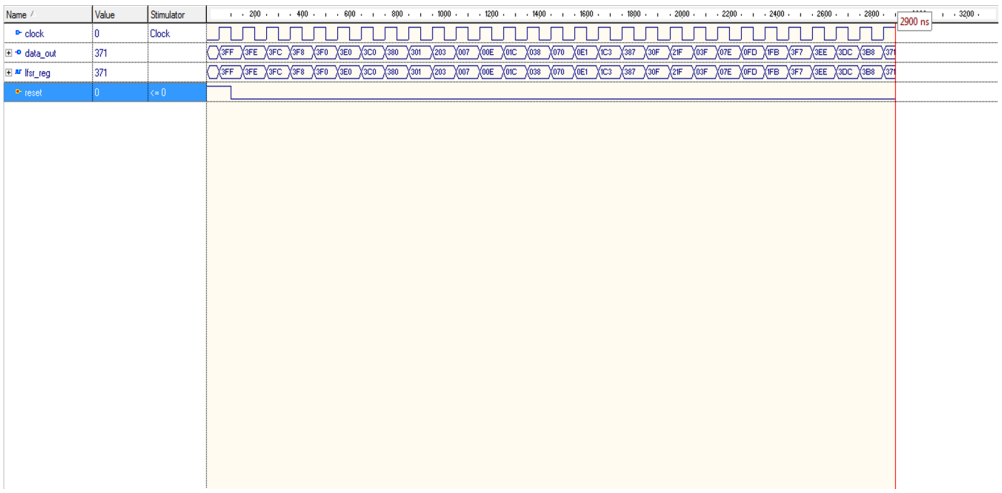

Figure 3. Universal BIST Array SOC Tester Simulation Results

Description : BIST Array Contains LFSR Shift Register to test the SOC Data

Simulation Results – Universal BIST Array SOC

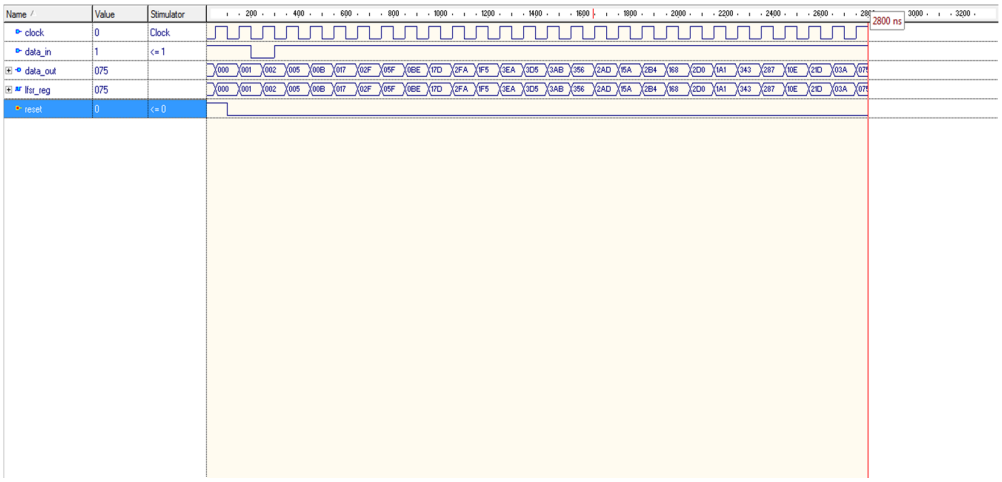

Figure 4. SimulationResultsBISTArraySOC Tester

Description: BIST Array SOC test the Mutliple SOC's At a Time

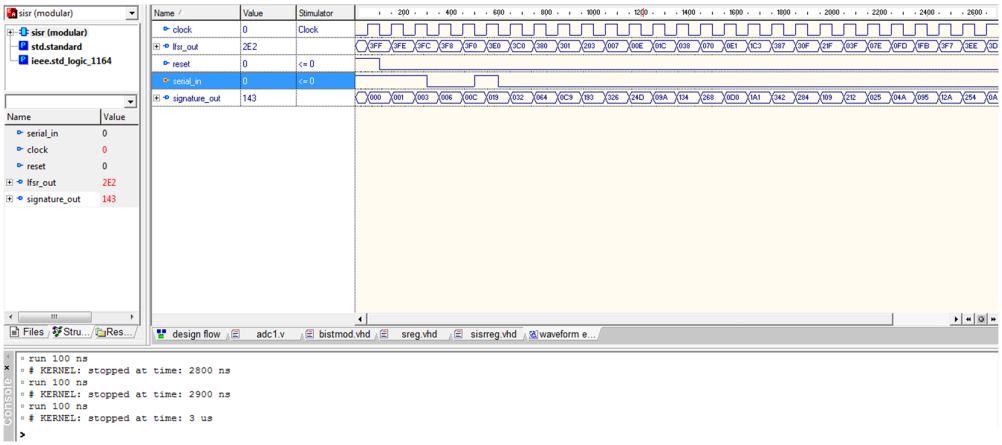

Figure 5. BIST Array SOC Simulation

CONCLUSION

Designed Boundary Scan SOC BIST Array Architecture and Implementation through FPGA for Testing Multiple SOC's at a time, So Due to this Speed of Testing is increased as well as more time save to test for Large Functional Design Blocks based Complex SOC's and ASIC's. also can easily deliver any complex SOC ASIC Products / Applications with High Quality and Reliability, Compatibility. For all IT Multinational Companies & Corporates, they are following the approach by meeting the deadline of Delivering product with in required amount of time. This IEEE Boundary Scan BIST Array SOC is very Suit for High Speed testing of Parallel Distributed Pipelined Computing Data / Cloud/Cluster/Big Data / Wireless NOC's/Cluster Computing / Grid Computing ASIC SOC's/ Entire Network Stations / Large Cities Electronic Design Data Servers.

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Prof.P.N.V.M Sastry Currently working with a Capacity of **Dean- IT EDA Software – R&D CELL & ECE** DEPARTMENT, He Did Master Degree In Science- M.S Electronics, Under Department Of Sciences, College Of Science & Technology AU -1998.Did PG Diploma In VLSI Design From V3 Logic Pvt Ltd B'Lore-2001, Did M.Tech (ECE) From IASE Deemed University-2005. Currently Pursuing (PhD)-ECE(VLSI) , **JNTU Hyderabad -2012** , Over **Past 16 years of Rich Professional** Experience with Reputed IT Software Industrial MNC's, Corporate –CYIENT (**INFOTECH), ISiTECH** as a **world top keen IT Industrial Software Specialist – World Top Software Engineering Team Leader(Level 6) Eng-Eng- HCM Electronics Vertical & Program Manager – MFG I/C,EDS,BT,NON BT Embedded Software ,Avionics & Automotive Hi-tech Software Engineering Verticals & Departments , Program Lead – Embedded & VLSI & Engineering Delivery Manager – IT Semiconductor Software Engineering Vertical ,at ISiTECH** , also worked with **Govt R&D, Industrial Organizations, Academic Institutions** of Comparative Designations & Rolls . His Areas Of Interest are VLSI –VHDL, Verilog HDL, ASIC, FPGA & Embedded Software Product Architectures Design & Coding Development .He mentored & Architecting Various Real Time, R&D ,Industrial Projects/Products related to VLSI & Embedded System Software & Hardware**..** His Key Achievements are Participated Various Top Class International IT MNC Delegates Board Meetings, IT Software MNC Board Meetings(Tier1/2 Level MRM-VP,COO Level) , Guided R&D ,Industrial , Academic Projects /Products –VLSI-ASIC,FPGA & Embedded & Embedded, VLSI Software Project &/ Program Management & Also Coordinated Various In House & External IT Project Workshops & Trainings At **CYIENT**(**INFOTECH)** as a I/C- MFG Eng Software Vertical , Also Participated Various National R&D Workshops, FESTS, FDP's &Seminars. Recently He Published Various national & International Journals.

G.Krishnaiah, Pursuing Ph.D from JNTU UNIVERSITY,Hyderabad, India. Currently working as a Professor, in the Department of Electronics and communication Engineering, Joginpally B.R Engineering college, Hyderabad, Telangana State, India. His carrier spans nearly 19 years in the field of teaching, administration, R&D, and Industry & Research. He has actively involved in organizing various conferences and work-shops. He has published over 4 international journal papers out of his research work. He presented more than 3 Research papers at various national and International conferences. He is currently a Life Member of ISTE, IETE,CSI, and Member of IEEE and MIE. He is also guiding the projects of U.G / P.G. students of various universities. His area of Research includes Digital Signal Processing; Image & Video signal Processing, Low power VLSI Design, Embedded systems, Wireless communication, Global Positioning systems and Pseudolite Systems.

Dr. D.N Rao B.Tech,M.E,Ph.D, principal of JBREC, Hyderabad. His carrier spans nearly three decades in the field of teaching, administration,R&D, and other diversified in-depth experience in academics and administration. He has actively involved in organizing various conferences and workshops. He has published over 11 international journal papers out of his research work. He presented more than 15 research papers at various national and international conferences. He is Currently approved reviewer of IASTED International journals and conferences from the year 2006. He is also guiding the projects of PG/PhD students of various universities.

Dr.Vathsal Currently working as a Professor & Dean- R&D & EEE,JBIET,He Obtained PhD from I.I.S.C,Bangalore,also Did Post Doctoral Research in DFVLR,Germany and NASA Goddard Space Flight Centre,USA,and also he worked with keen Designations Scientist E,F,G from Reputed Govt R&D Industry Organizations over past years and closely worked with Dr.A.P.J Abdul Kalam He Published lot of various national, international journals & conferences, He guiding 5 PhD Students from Various universities. He Got Prestigious awarded as a Noble Son of India.